INTERRUPT PROCESSING IN A DATA PROCESSING SYSTEM

Abstract of the Disclosure

The present invention relates generally to interrupt processing. One embodiment relates to a method for executing an interrupt in a data processing system including fetching a conditional store instruction that is conditional upon a reservation, receiving notice that an interrupt is pending, invalidating a reservation in response to receiving the notice, and processing the interrupt. Invalidating the reservation allows the conditional store instruction to finish in a predetermined amount of time and properly update an architectural state of the processor. Therefore, interrupt latencies (the amount of time between receiving and processing an interrupt) corresponding to the conditional store instruction can be bounded. The method may be used in a single processor or multi-processor data processing system, wherein each processor includes a reservation register. Furthermore, each processor may include both a completion unit for storing instructions in the order they are issued and a store queue within a load/store unit.